(12) UK Patent Application (19) GB (11) 2 081 018 A

(21) Application No 8123089
(22) Date of filing 27 Jul 1981
(30) Priority data
(31) 55/105308
(32) 31 Jul 1980
(31) 55/105307
(32) 31 Jul 1980
(31) 56/018228
(32) 10 Feb 1981
(33) Japan (JP)
(43) Application published
10 Feb 1982
(51) INT CL³
H01L 27/13 49/02
(52) Domestic classification
H1K 11A3 11C1A 11C1B
11C4 11D3 11D 1CA
4C11 4C14 5E9 9C2 9D1
9N3 9R2 GAA
G5C A310 A342 HG
(56) Documents cited
GB 2066545A
GB 2005073A
GB 1488307
GB 1465244
GB 1465840
GB 1417055
GB 1415455
GB 1462238
GB 1325668
(58) Field of search
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(54) Active Matrix Assembly for Display Device

(57) An active matrix assembly for a display device comprises a first thin layer of silicon (27), an insulating layer (30) on the first layer of silicon, and a second thin layer of silicon (29) on the insulating layer. The first and second layers of silicon constitute a channel region (28) and a gate, respectively, of a thin film transistor and the electrodes of a capacitor, whilst the insulating layer constitutes the dielectric of the capacitor and the gate insulation of the transistor. The transistor addresses signals from a data line to the capacitor which drives a liquid crystal display.

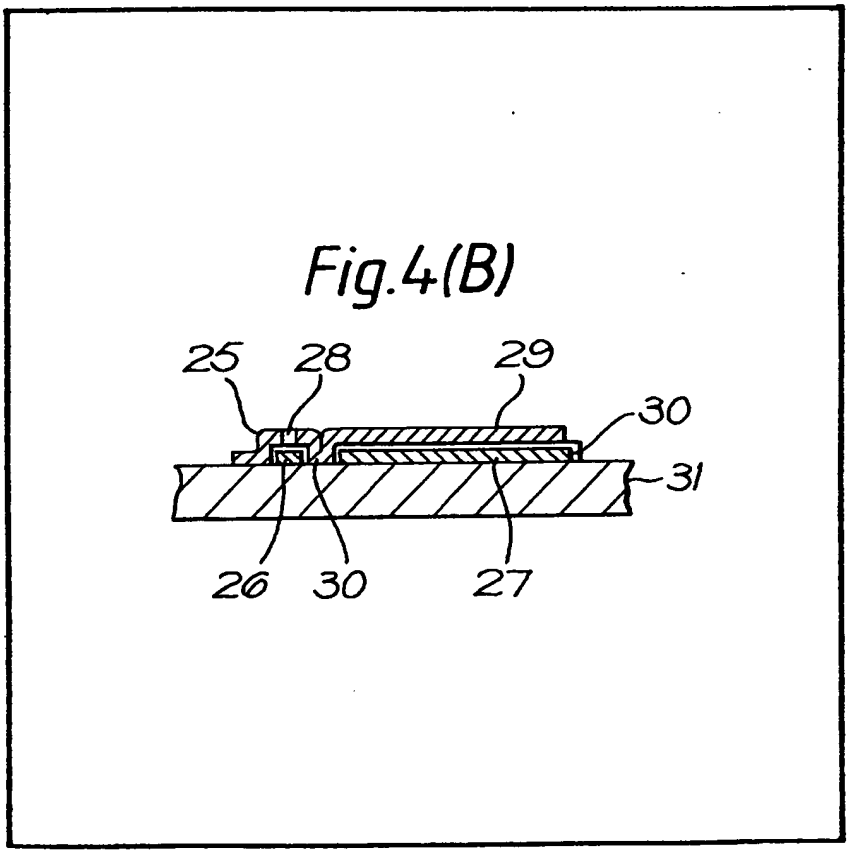

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Fig.1.

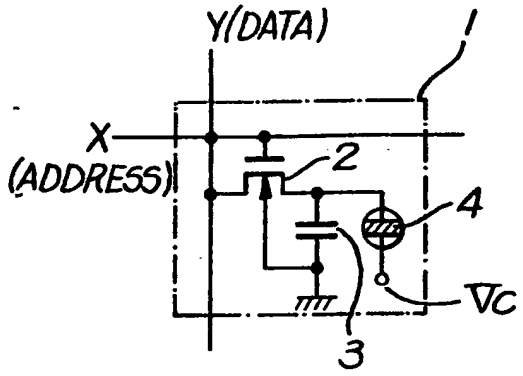


Fig.2.

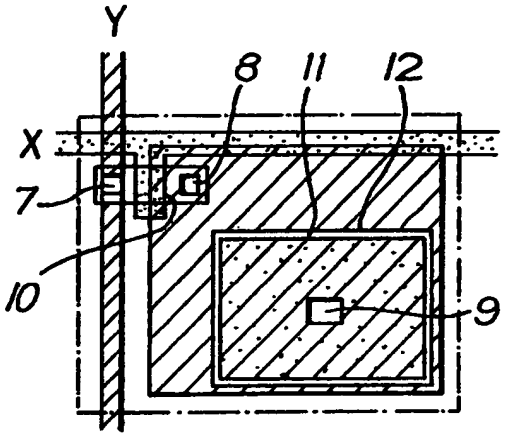


Fig.3.

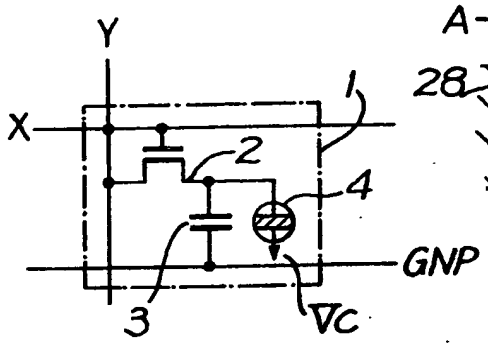


Fig.4(A)

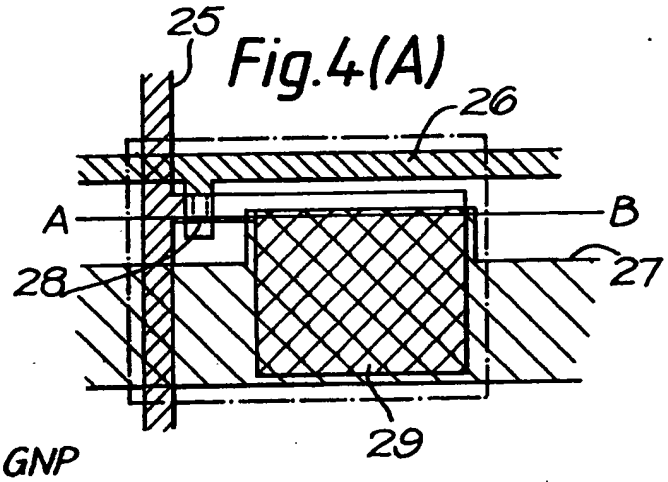


Fig.4(B)

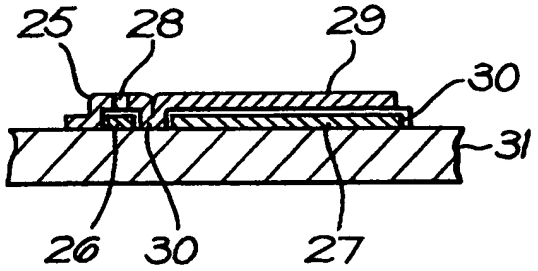


Fig.5.

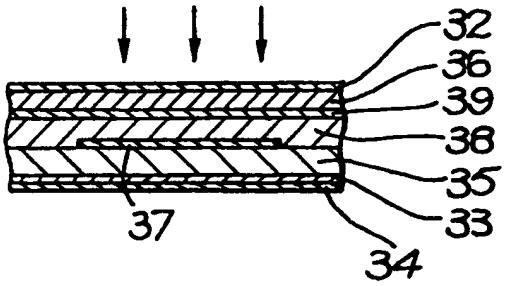


Fig.6.

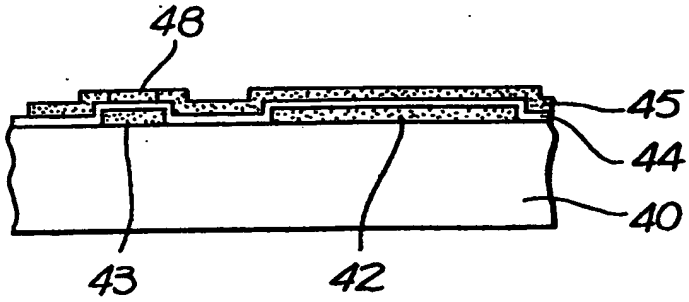


Fig.7.

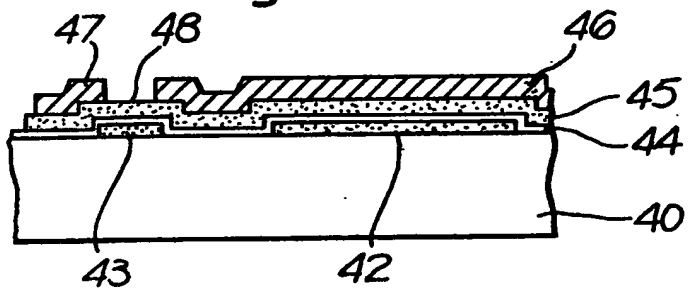


Fig.8.

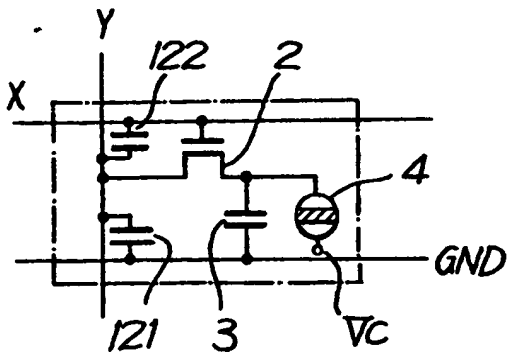


Fig.9(A)

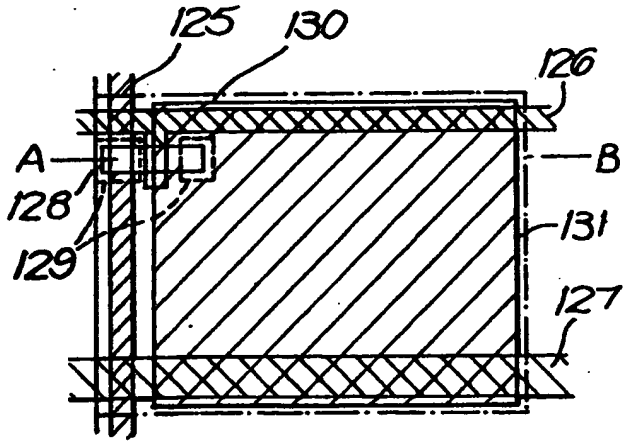


Fig. 9(B)

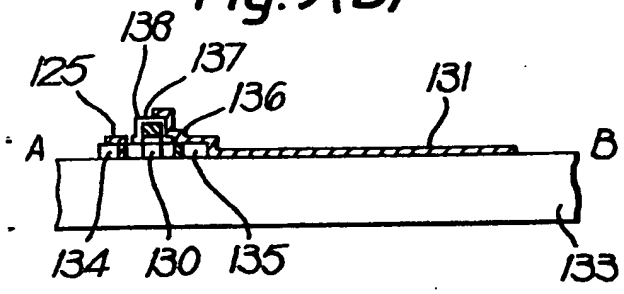


Fig. 10(a)

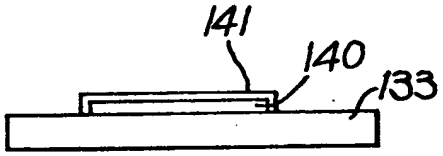


Fig. 10(b)

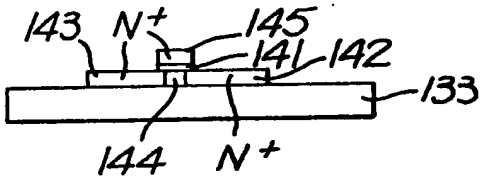


Fig. 10(c)

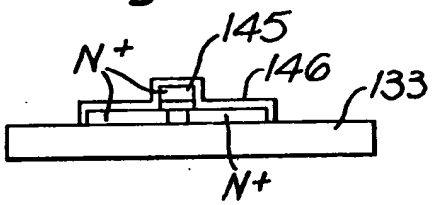


Fig. 11.

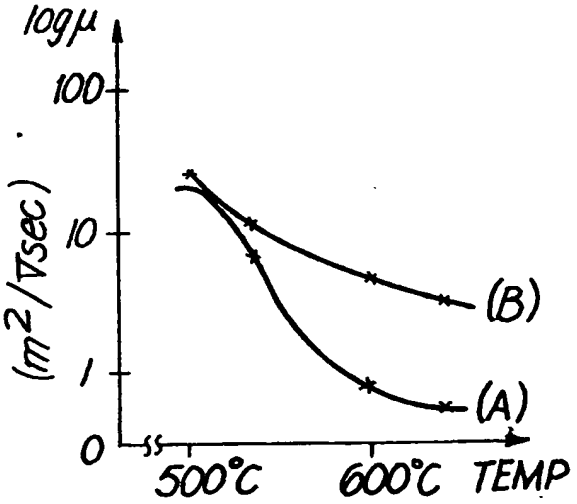


Fig. 12.

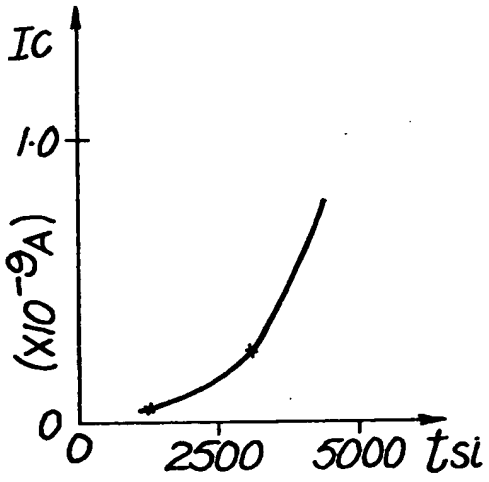


Fig.13.

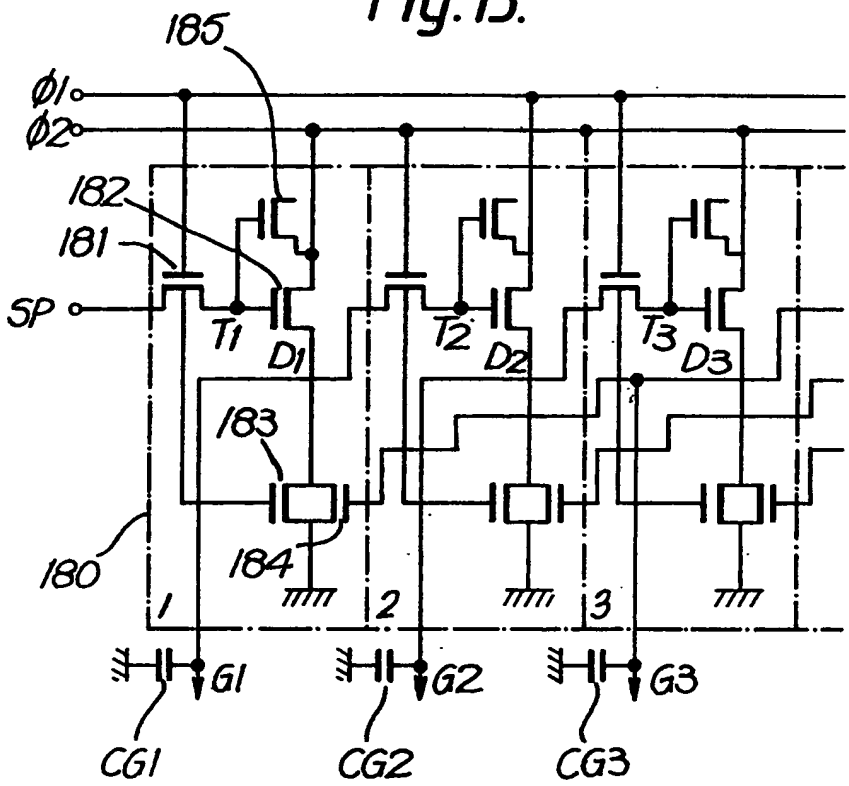
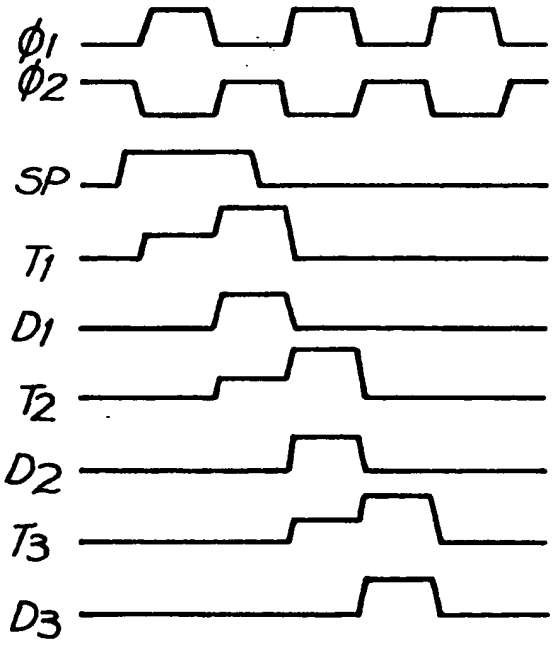

185
φ1
φ2
182
181
SP
T1
D1
T2
D2
T3
D3
183
184
180
1
2
3
G1
G2
G3
CG1
CG2
CG3

Fig.14.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SP
T1
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D3

Fig.15.

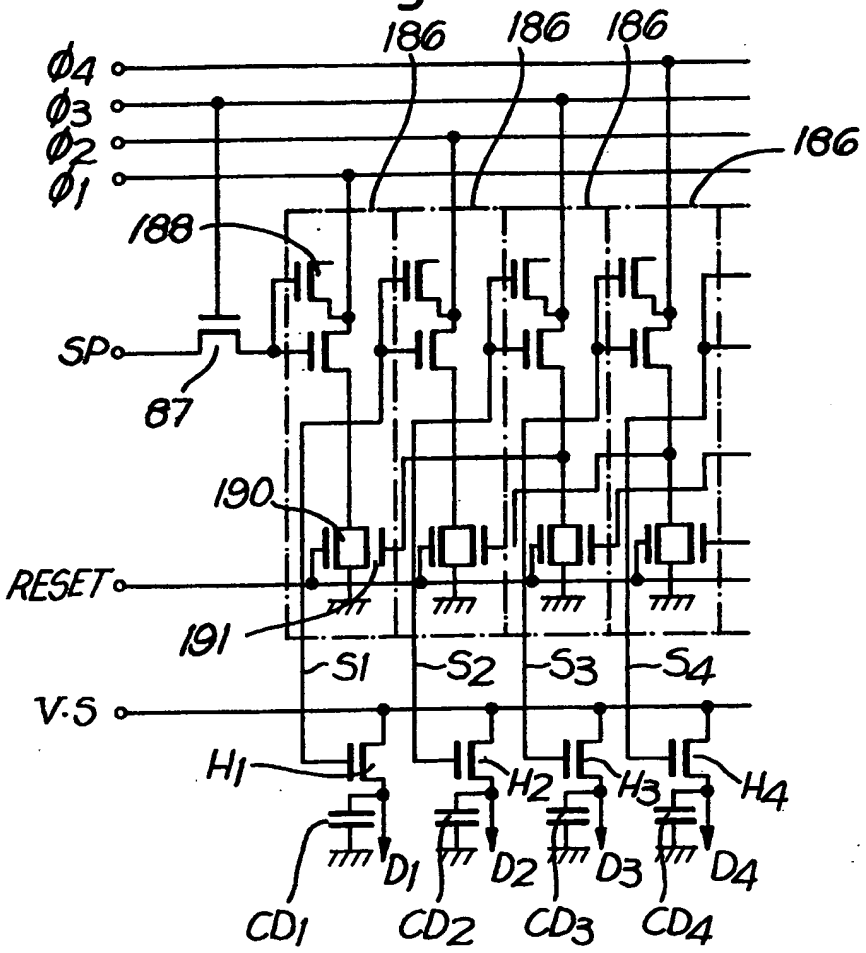

186
186
186
186
φ4
φ3
φ2
φ1
188
SP
87
190
RESET
191
S1
S2
S3
S4
V.S
H1
H2
H3
H4
D1
D2
D3
D4
CD1
CD2
CD3
CD4

Fig.16.

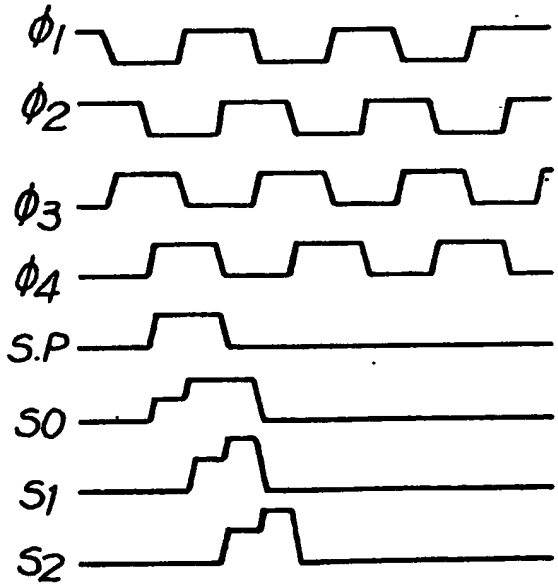
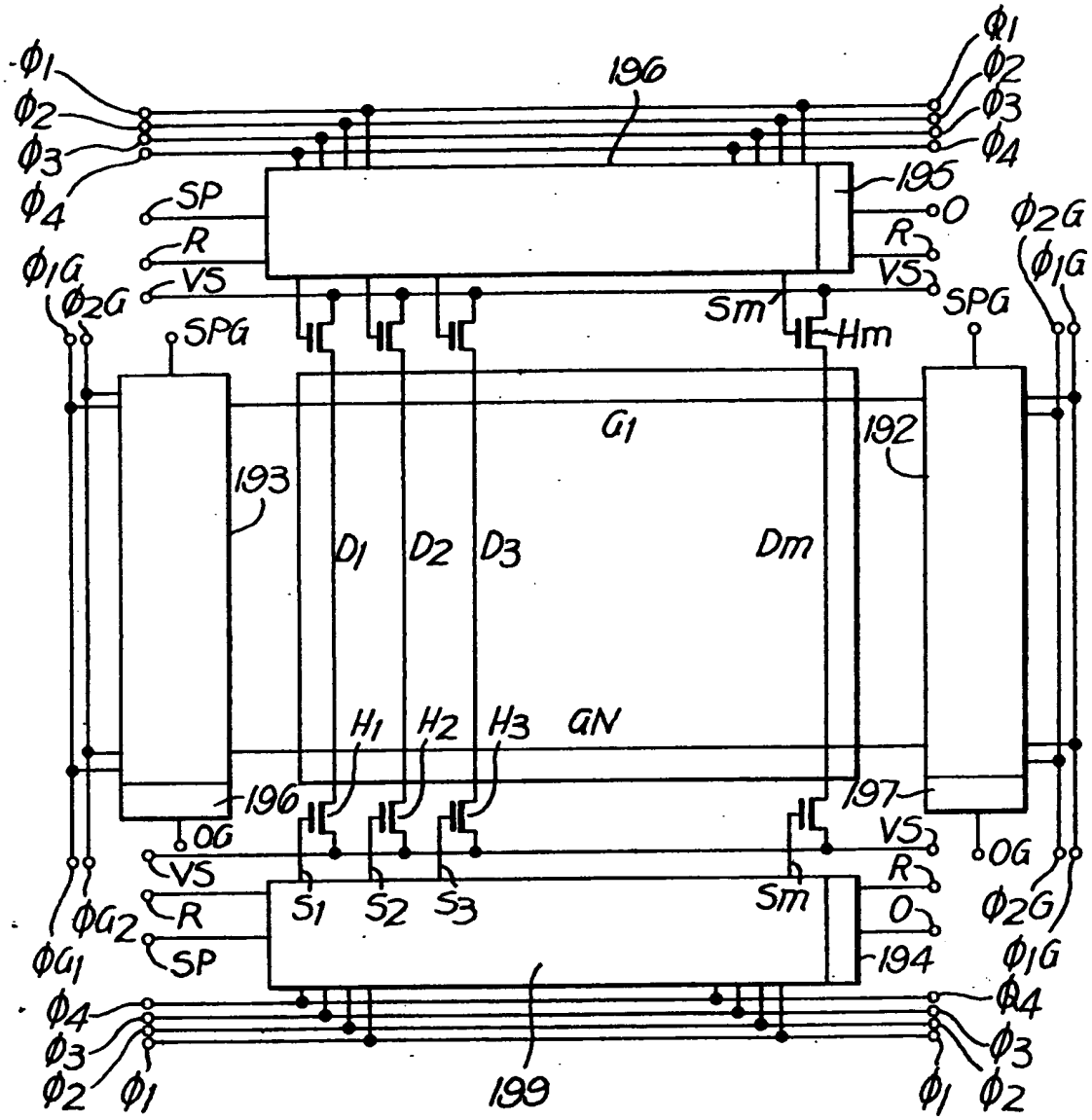

φ1
φ2
φ3
φ4
S.P
S0
S1
S2

Fig. 17.


φ1
φ2
φ3
φ4
196
195
SP
R
VS
O
φ1G
φ2G
SPG
Sm
Hm
G1
192
193
D1
D2
D3
Dm
H1
H2
H3
GN
197
OG
S1
S2
S3
194
199

SPECIFICATION

Active Matrix Assembly

This invention relates to active matrix assemblies, for example, for display devices using MIS (metal-insulator-semiconductor) transistor arrays.

Display devices or display panels with active matrix assemblies have been attracting much attention in that the size of the matrices can be increased and hence the panels can be made relatively large in size with a greater number of display elements or dots. Paticularly, application of an active matrix assembly to display television pictures is now under consideration since passive displays, such as liquid crystal displays, have limitations imposed by the drive duty in a dynamic system.

According to the present invention there is provided an active matrix assembly including a thin layer of silicon which defines a channel region.

The assembly may include a first thin layer of silicon, a first insulating layer on said first layer of silicon, and a second thin layer of silicon.

Said first and second layers of silicon may constitute a channel region and a gate, respectively, of a transistor. Alternatively said first and second layers of silicon may constitute a gate and a channel region, respectively, of a transistor.

Said first insulating layer preferably constitutes a dielectric of a capacitor, and said first and second layers of silicon constitute electrodes of the capacitor.

One embodiment of the assembly may include a second insulating layer on said second layer of silicon and wiring material on said second insulating layer, said second insulating layer constituting a dielectric of a capacitor, said second layer of silicon and said wiring material constituting electrodes of the capacitor.

Said assembly may be formed by a low temperature process at a temperature of 600°C or less, said first insulating layer comprising an oxide film formed by an O_2 plasma technique. Alternatively said assembly may be formed by a low temperature process at a temperature of 600°C or less, said first and/or second insulating layer comprising an oxide film formed by an O_2 plasma technique.

In a preferred embodiment said layer of silicon which defines the channel region is locally annealed by a laser beam or electron beam. Thus said layer of silicon which defines the channel region may be formed by a reduced pressure chemical vapour deposition technique at a temperature of 600°C or less.

Preferably said layer of silicon which defines the channel region has a thickness of 3,700Å or less. An active matrix assembly according to the present invention may include a transparent substrate and a transparent liquid crystal driving electrode on said transparent substrate. Thus the assembly may include wiring material for a data line, said transparent liquid crystal driving electrode being made of a material which is the same as said wiring material.

Said transparent liquid crystal driving electrode may be made of a Si_nO_2 film, a metal film having a thickness of 500Å or less, or a thin film of silicon.

In an alternative process for making an active matrix assembly according to the present invention, said assembly is formed by a high temperature process at a temperature of 600°C or higher, said first insulating layer comprising a thin thermal oxide film of silicon. The assembly may be formed by a high temperature process at a temperature of 600°C or higher, said first and/or second insulating layer comprising said first and/or second layer of silicon respectively which has been thermally oxidised.

The assembly preferably includes a liquid crystal segment drivable in a twisted nematic mode.

In one embodiment the assembly includes a substrate on which the active matrix assembly is formed together with at least one peripheral drive circuit, said at least one peripheral drive circuit including non-inverting ratioless shift registers.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:

Figure 1 is a schematic diagram of a cell of a conventional active matrix assembly;

Figure 2 is a plan view showing the structure of the cell of Figure 1;

Figure 3 is a schematic diagram of a cell of one embodiment of an active matrix assembly according to the present invention;

Figure 4 consists of Figures 4(A) and 4(B) which are plan and sectional view (on line A—B of Figure 4(A)) respectively of the cell of Figure 3;

Figure 5 illustrates a liquid crystal display device incorporating an active matrix assembly according to the present invention;

Figure 6 is a cross-section of a cell of another embodiment of an active matrix assembly according to the present invention;

Figure 7 illustrates a modification of the cell of Figure 6;

Figure 8 is a schematic diagram of a cell of another embodiment of an active matrix assembly according to the present invention;

Figure 9 consists of Figures 9(A) and 9(B) which are plan and sectional views (on line A—B of Figure 9(B) respectively of the structure of the cell of Figure 8;

Figure 10 is used to illustrate processes for manufacturing the cell of Figure 9;

Figure 11 illustrates graphically the relationship between mobility and temperature of formation of a first thin layer of silicon by the process described in relation to Figure 10;

Figure 12 is a graph illustrating the relationship between OFF leakage current as a function of thickness of the first thin layer of silicon;

Figure 13 illustrates a drive circuit for a gate line of an active matrix assembly according to the present invention;

Figure 14 is a timing chart to illustrate the

operation of the driving circuit of Figure 13;

Figure 15 illustrates the drive circuit for a data line of an active matrix assembly according to the present invention;

Figure 16 is a timing chart to illustrate the operation of the drive circuit of Figure 15; and

Figure 17 is a circuit diagram of a complete active matrix assembly according to the present invention.

Throughout the drawings like parts have been designated by the same reference numerals.

Figure 1 illustrates a cell 1 of a conventional active matrix assembly. An address line X is connected to a gate of a transistor 2. When the transistor 2 is rendered conductive, a signal from a data line Y is stored as an electric charge on capacitor 3. At the same time, the signal stored in the capacitor 3 drives a liquid crystal display segment 4. A common electrode signal is indicated by Vc. Since the liquid crystal display segment undergoes relatively little charge leakage, it is sufficient to store the charge on the capacitor 3 for only a relatively short period of time. Conventionally, the transistor 2 and the capacitor 3 are manufactured in the same manner as conventional integrated circuits.

Figure 2 illustrates the structure of the cell of Figure 1 made by silicon gate process. A transistor 10 and a capacitor 11 are formed on a single crystal silicon wafer substrate. The address line X and an upper electrode 12 of the capacitor are made of polycrystalline silicon (polysilicon), and the data line Y and a liquid crystal driving electrode 13 are made of aluminium. The substrate and the aluminium, and the polycrystalline silicon and the aluminium are connected together through contact holes 7, 8, 9.

An active matrix assembly formed by this conventional integrated circuit technique has the following disadvantages.

First, since the active matrix assembly is manufactured at the same time as other integrated circuits, the manufacturing process is relatively complicated and costly, and yield becomes poor due to junction charge leakage between the silicon substrate and the other elements, with a resulting increased overall cost of manufacture. Particularly, leakage current flow across the junction between the silicon substrate and the diffusion layer which composes the source and drain of the transistor, the leakage current being substantially dependent on defects in the silicon substrate which is a single crystal. Such a leakage current is several hundreds of picoamps (PA) or less for a single cell and it is extremely difficult to eliminate leakage current completely when there are tens of thousands of such cells. The leakage current causes the charge stored on the capacitor 3 to discharge, lowering the degree of contrast of any display produced.

A second disadvantage is that since the liquid crystal driving electrode 13 is of aluminium and does not transmit light, a light-transmitting arrangement using a conventional FE liquid crystal display segment is not feasible and hence application is limited to display segments in which light is reflected from a surface of the aluminium liquid crystal driving electrode, such as a guest-host liquid crystal display segment or a DSM liquid crystal display segment. The guest-host liquid crystal display segment, however, has a reduced degree of contrast, and a DSM liquid crystal display segment is greatly dependent on viewing angle.

A further disadvantage is that the light which enters the substrate through gaps in the liquid crystal driving electrode 13 forms electron-hole pairs which migrate to produce a photo current, discharging the capacitor and this again lowers contrast.

Figure 3 illustrates a cell of an active matrix assembly according to the present invention which is basically the same as the cell 1 shown in Figure 1 except that there is a ground line GND for the capacitor 3.

Figure 4 shows the structure of the cell of Figure 3, Figure 4(A) being a plan view showing an address line 26 connected to a gate of a channel 28 of a transistor having a source constituted by a data line 25 and a drain constituted by a driving electrode and a capacitor electrode 29. A ground line 27 is constructed in the same fashion as the address line 26 and provides a capacitance between itself and the electrode 29.

Figure 4(B) is a cross-sectional view taken along the line A—B in Figure 4(A). One process for the manufacture of the structure shown in Figure 4 is as follows. A layer of polycrystalline silicon about 3000Å in thickness is grown on a substrate 31 of a high melting point glass such as, for example, quartz, and thereafter P ions are implanted over the entire surface to form an N-type polycrystalline silicon layer. A thin film of SiO_2 may be formed in advance, if necessary, for improved intimate bonding contact. Next a gate 26 and a capacitor electrode 27 are formed by photo-etching a film 30 of SiO_2 about 1500Å in thickness if grown by a thermal oxidation technique to form a gate insulating film and a dielectric film of the capacitor. A second layer of polycrystalline silicon is then formed and patterned by a photoetching technique. Then, with a photoresist mask placed over the second layer of polycrystalline silicon, P ions are implanted over those areas except for the channel 28, thereby forming source and drain electrodes, the data line 25 and a driving electrode for the liquid crystal segment which driving electrode doubles as a capacitor electrode. Since at this stage the transistor has poor threshold and conductance performance, the channel 28 or the overall assembly are illuminated uniformly with laser light to fuse and solidify the polycrystalline silicon in a relatively short period of time for grain growth, whereby performance of the transistor can be improved. This procedure is the so-called "laser annealing" technique.

Figure 5 is a schematic cross-sectional view of a liquid crystal display device having an active

matrix assembly according to the present invention. A liquid crystal display segment 38 is sandwiched between a quartz substrate 35 carrying a polycrystalline silicon electrode 37 thereon and a glass layer 36 with a common electrode 39 of, for example NESA (Trade Mark). This arrangement is sandwiched between polarizing plates 32, 33 with a reflector 34 attached to the plate 33. Incident light (indicated by arrows) from above passes substantially through the electrode 37 and is reflected by the reflector 34 before the light is sensed by the human eye. Such an arrangement allows ordinary FE liquid crystal display segments (e.g. those operating in the twisted nematic liquid crystal mode) to be employed which provide a high degree of contrast and a wide angle of vision.

The cell shown in Figure 4 employs a transparent electrode but an aluminium electrode may be used. Moreover, the transistor may be formed on the silicon substrate whereon a thermal oxide film is provided, instead of the substrate of quartz.

Figure 6 is a cross-sectional view of a cell of another embodiment of an active matrix assembly according to the present invention, the cell being constructed on an ordinary glass substrate 40. A first polycrystalline silicon layer is formed on the glass substrate 40 by a low temperature film growth technique such as a sputtering technique, or plasma vapour deposition (CVD) technique, and then P ions or B ions are implanted all over silicon layer. A gate 43 and a capacitor electrode 42 are formed by a photo-etching technique of the silicon layer. An insulating film 44 of, for example, SiO_2 is then formed by a low temperature film growth technique. A second polycrystalline silicon layer 45 is formed at a low temperature, which serves as the source and drain of the transistor, and a capacitor and a driving electrode. The second silicon layer is either not doped, or B ions are implanted to an extent sufficient for threshold enhancement. P ions are implanted in the source and drain and the area that defines the capacitor and the driving electrode but not in the region of a channel region.

Thereafter, a localized portion of the whole assembly is illuminated with a laser beam for laser annealing. The laser beam is partially absorbed in the first and second silicon layers, but passes through the glass substrate 40. Thus annealing without adversely affecting the glass substrate is possible when treated with an appropriate energy laser beam applied for a suitable period of time (determined by the pulse interval of a pulse laser, and by a scanning speed with a CW laser) and activation of ion-implanted impurities in the first silicon layer and for good grain growth (particularly in the region of the channel 48) and activation of ion-implantation impurities in the second silicon layer. Thus an active matrix assembly of this construction has the advantage that less costly glass can be used for the substrate because it is less affected by laser annealing than by an ordinary annealing technique. Moreover, simultaneously laser annealing activates the impurities and grows the grains of the silicon layers, especially when made of polycrystalline silicon, for improving transistor characteristics and in particular ion mobility.

As shown in Figure 7, aluminium may be deposited and patterned by a photo-etching technique to form source and drain electrodes 46, 47. The aluminium and silicon are subjected to heat treatment or illuminated with a weak laser beam to obtain good contact between them.

The active matrix assemblies according to the present invention and described above have polycrystalline silicon electrodes on a transparent substrate with the following advantages. The manufacturing process is relatively simple (three or four photo-etching steps are sufficient) and less costly than conventional processes requiring six photo-etching steps. P—N junctions are much fewer than with a bulk silicon process such as described in relation to Figure 2. There is only slight junction current leakage and there is an increased manufacturing yield. The liquid crystal driving electrode is virtually transparent, thus enabling the display device shown in Figure 5 to have an increased viewing angle and increased contrast. 90% or more of the incident light passes through the display device and an interval of diffusion of carriers in the polycrystalline silicon layers is relatively short, so that substantially no photo current is generated whereby the problem of leakage current due to incident light is overcome. This leakage current due to incident light may be reduced to 10 PA or less when the incident light is 10^4 lux and yet the display remains visible.

An active matrix assembly according to the present invention may be used in the construction of a portable liquid crystal display television of low power consumption. A television screen can be manufactured which gives a high degree of contrast even when watched outdoors under relatively intense sunlight.

Figure 8 is a schematic diagram of a cell of another embodiment of an active matrix assembly according to the present invention and is a modification of the active matrix assembly of Figure 4. The active matrix assembly shown in Figure 8 differs from that shown in Figure 4 in that a capacitor 121 is connected between the data line Y and the ground line GND and a capacitor 122 is connected between the data line Y and the address line X serving to sample and hold display data input. The ground line GND is held at constant bias voltage with a bias level or a signal level selected as desired.

Figure 9 shows the structure of the cell of Figure 8, Figure 9(A) being a plan view and Figure 9(B) being a cross-sectional view. On a transparent substrate 133, there is formed a first thin layer 128 of silicon which defines the source, drain and channel of a transistor, a second thin layer 126 of silicon or its equivalent line layer which defines a gate line serving as the gate of the transistor, a ground line 127, and a data line

125 made of a transparent low-resistance material such as a NESA (Trade Mark) film of S_nO_2 or a metal layer having a thickness of several hundreds Å or less, there being contact holes 129 through which a liquid crystal driving electrode 131 and the silicon layers are electrically connected together. An area wherein a ground line 127 and the liquid crystal driving electrode 131 overlap constitutes the capacitor 3. A source 134 and a drain 135 of the transistor are formed by N^+ diffusion (P^+ diffusion if a P type channel is to be formed). A channel 130 is disposed below a gate electrode 138 with a gate insulation film 136 interposed therebetween. The gate electrode 138 is surrounded by an insulation film 137 such as an oxide film.

Figure 10 illustrates a process of manufacturing the cell shown in Figure 9. There are two practical manufacturing processes available, one being a low-temperature process and the other being a high-temperature process. The low-temperature process uses a relatively inexpensive glass as the transparent substrate 133, for example, a high melting point glass such as Pyrex (Trade Mark) or Corning (Trade Mark) glass and is performed at a temperature of 600°C or less. According to the low-temperature process, a thin layer 140 of silicon is formed on the substrate 133 by a CVD technique such as a plasma CVD technique or a reduced-pressure CVD technique or a sputtering technique and then the thin layer 140 of silicon thus formed is patterned as desired by a photo-etching technique. Thereafter, its surface is oxidised in an O_2 plasma atmosphere. In practice, an equivalent insulation film may be deposited by a CVD technique. As a result, an oxide film 141 which will serve as a gate insulation film is formed on a thin film 140 of silicon (Figure 10(a)). Subsequently, a second thin layer 145 of silicon is deposited in the same manner as the first thin layer of silicon, and is patterned by a photo-etching technique. Then the oxide film 141 is etched with the second thin layer 145 of silicon acting as a mask thereby to define a gate insulating film. At the same time, a window opening is made preparatory to diffusion, and ions are implanted whereupon a source 142, a drain 143 and a channel 144 are formed (Figure 10(b)). Thereafter, the assembly is subjected again to a plasma treatment in an O_2 atmosphere to form a plasma oxide film 146 on the surface, and is annealed at a temperature in the range of 400°C to 600°C (Figure 10(C)). The foregoing process is characterised in that the thin layer 140 of silicon is oxidised directly by a plasma treatment technique and the gate insulating film of a transistor and the dielectric film of a capacitor produced by the process are more advantageous than oxide films produced by CVD techniques in that mobility is improved and reliability is increased.

The high-temperature process is based on using a transparent substrate having a melting point of 600°C or higher, and includes a step to be performed at a temperature exceeding 600°C. Since the process involves annealing at a high temperature, mobility and reliability of transistors produced are improved. The high-temperature process will be described with reference to Figure 10 again as the structure of a transistor formed is the same as that of a transistor produced by the low-temperature process. In Figure 10(a), a first thin layer of silicon is formed on a transparent substrate by a reduced pressure or normal pressure CVD technique and is patterned to provide the thin film 140 of silicon. Then, it is thermally oxidised at a temperature between 900°C and 1100°C to form the oxide film 141. Subsequently, as illustrated in Figure 10(b), the second thin layer 145 of silicon is deposited in the same manner as the first thin layer of silicon, and the second thin layer 145 of silicon is then patterned and used as a mask to etch the oxide film 141. N^+ or P^+ impurities are pre-deposited, or ions are implanted without etching the oxide film 141 to form the source 142 and the drain 143. Thereafter, the thermal oxide film 146 which will serve as the dielectric film of the capacitor 3 is formed in the same manner as the gate insulating film shown in Figure 10(c).

With the arrangement illustrated in Figure 9, the gate insulating film of the transistor is self-aligned by forming the first thin layer of silicon on a thin oxide or silicon film, and such self-alignment reduces parasitic capacitance thereby to prevent reduction of mobility and speed as compared with the conventional single crystalline bulk silicon process already described in relation to Figure 2. In addition, the oxide film on the second thin layer of silicon or an insulating film thereon is used as the dielectric film of the capacitor 3 and the capacitors 121, 122 for sampling and holding the data line. According to the conventional bulk silicon process, the gate insulating film of the transistor and the capacitor entirely use a thermal oxide film of bulk silicon. However, where doping of impurities results in gate self-alignment as shown in Figure 10(b), high density impurities cannot go under the second layer of silicon which will constitute one electrode of the capacitor. The capacitor thus formed is unstable and difficult to use. For the capacitor to be used, an additional step is necessary to dope the lower capacitor electrode heavily with impurities as with the bulk silicon. As shown in Figure 9, therefore, the dielectric film which will form the capacitor 3 is formed on the second thin layer of silicon, thereby to simplify the manufacturing process and render the capacitor stable.

The manufacturing steps subsequent to the step shown in Figure 10(c) are substantially the same in either the low-temperature or the high-temperature process. Contact holes are formed to provide contact between the line, the first and the second layers of silicon, and a material which serves as the line and transparent drive electrodes, for example, a NESA (Trade Mark) film or a metal film having a thickness of several

hundreds Å or less are formed by a sputtering technique or an evaporation technique and patterned by a photo-etching technique. Where a material such as NESA (Trade Mark) film is employed which is difficult to get in direct contact with the thin film of silicon, a substance such as, for example, gold or nickel-chromium is applied in appropriate areas for ease of contact.

Since the transistor prepared according to the process of the present invention has reduced mobility and increased OFF leakage current as compared with a transistor formed by the bulk silicon process, care should be taken to avoid the difficulties referred to hereafter. The curve (A) shown in Figure 11 illustrates mobility of a transistor at 10 volts which is formed by the high-temperature process where the first thin layer of silicon is deposited by a reduced-pressure CVD technique at different temperatures. It has been found experimentally that mobility abruptly improves when the deposition temperature drops below 600°C. Accordingly, improved mobility and reliable response can be obtained by forming the first thin layer of silicon by a reduced-pressure CVD technique at a temperature of 600°C or less.

Figure 12 is a graph illustrating OFF leakage current IL of a transistor at 10 volts as a function of the thickness of the first thin layer of silicon. It has been found by experiment that the leakage current is reduced below 500 PA (5×10^{-10} amps) or less to enable trouble-free usage when the thickness of the first silicon layer is 3,700 Å or less.

The low-temperature and high-temperature processes described above result in a relatively large reduction in mobility. It is therefore considered that improvement may be obtained by annealing the first thin layer of silicon with a laser electron beam applied locally at a high temperature with care being taken not to adversely affect the substrate. Curve (B) in Figure 11 shows improved mobility of a transistor achieved by having a thin silicon film prepared as with that of curve (A) and illuminated with a laser beam of 0.12 mJ per pulse and a pulse width of S onsec by a Q switch method. Furthermore, mobility of a transistor according to the low-temperature process which has been formed by deposition on a high-melting point glass at 500°C to 540°C and then laser-annealed under the same conditions coincides substantially with that indicated by curve (B) in Figure 11. From the foregoing, it will be seen that localised annealing by means of a laser or electron beam is effective in either the low-temperature process or high-temperature process already discussed above.

One method has already been described for making the active matrix assembly of Figure 4 but it can also be made by a low-temperature process. In such a process, the gate of the transistor is defined by a first layer of silicon and the channel of the transistor is defined by a first layer of silicon, such that heavy diffusion is possible as desired on both the thin layers of silicon, and a gate oxide film which is formed by oxidising the first layer of silicon or the gate insulating film on the first layer of silicon is available as a dielectric layer of a capacitor. Therefore, only one step suffices for forming the oxide film. The first layer of silicon provides address and ground lines, and the second layer of silicon provides a data line, with the result that no step is necessary to deposit wiring material and to pattern the latter by photo-etching, which is the case with the arrangement shown in Figure 9. Furthermore, a silicon film is used as a transparent electrode for driving the liquid crystal display segments, the silicon film being sufficiently transparent if it is 3000 Å or less in thickness.

The active matrix assembly shown in Figure 9 which employs transparent liquid crystal driving electrodes on a transparent substrate, can provide a much greater degree of contrast than that made by the bulk silicon process already described, since the latter has an opaque substrate and hence cannot rely on FE (TN) liquid crystal segments which provide maximum contrast.

Where an opaque substrate or an opaque driving electrode is used with an active matrix assembly according to the present invention, no substantial contrast improvement is attained if Guest-Host display segments or DSM type liquid crystal display segments are employed as with the conventional bulk silicon process. However, the active matrix assemblies of the present invention still serve to simplify manufacture, increase yield for each step; and prevent elimination of the display due to current leakage due to incident light.

With a substrate of, for example, glass or quartz, a display panel can be assembled more easily than a conventional panel in which one electrode of a liquid crystal segment is formed by the bulk silicon process. If a single crystal silicon wafer is used for the transparent substrate 35 of Figure 5, it tends to be easily cracked along a cleavage plane when subjected to force during assembly. In addition, the silicon wafer may warp to a large extent when thermally treated for 10 μm or more while the liquid crystal segment 38 has a thickness of from 5 μm to 15 μm. With liquid crystal segments having a constant thickness, the assembly operation becomes complicated.

The liquid crystal segments are insufficiently sealed at a high temperature because they and the glass above them have different coefficients of expansion. The foregoing difficulties are all overcome by liquid crystal display devices shown in Figure 5 in which glass or similar material is used as a substrate for the lower electrode. Thus, the display panel can be assembled relatively easily with good yield in the same manner as ordinary liquid crystal display panels.

The capacitor 3 serves to hold display data for the active matrix assembly for a given period of time, say about 16 msec. for a television picture image as an example. Where the transistor 2 has a leakage current of 100 PA or less at 10 volts,

the capacitor 3 should have a capacitance of from 0.5 PF to 1 PF. When the thickness of the liquid crystal segment is 10 μm or less, especially with a high specific inductive capacity of 10 or greater, the liquid crystal segment itself has a capacity of 0.5 PF or greater, with the result that the capacitor 3 can be dispensed with together with the ground line GND so that the effective area of the liquid crystal display device is increased giving improved contrast and the reduced number of elements increases yield. The sampling and holding capacitance of the data line Y is mainly constituted by the parasitic capacitor 122 (Figure 9) at the junction between the data address lines.

The active matrix assembly according to the present invention may include external drive circuits, that is, a shift register and a sampling and holding circuit, to be formed on the same substrate.

Figure 13 shows a drive circuit for a gate line. A plurality (*n*) of shift register cells 180 are provided, eachcell comprising four transistors 181—184 and a single bootstrap capacitor 185. A potential "1" applied to a start pulse input Sp is transferred in successive synchronism with two-phase clock signals φ_1, φ_2. Outputs D_1 to D_n of the shift register cells 180 are applied to gate lines for successive selection of the gate lines as illustrated in Figure 14. The transfer gate transistor 181 is connected as the input of each of the shift register cells. The potential "1" is stored initially at T_1 to T_N and written in D_1 to D_N by way of the bootstrap capacitors. If it were not for the transfer gate transistors D_1 and T_2, D_2 and T_3, etc. would be short-circuited, thus requiring the bootstrap capacitance to be much larger than gate line capitance CG1 to CGn. The pattern would therefore be enlarged and reduced yield would result. For D_1 to D_N to be dicharged to level "0", it is only necessary to connect T_3 to the transistor 184. Where the shift register is actuated at a low frequency, however, since it malfunctions even if a slight current leakage occurs, the transistor 183 as a potential-fixing transistor is included to restore to level "0" for each half period of the clock signals so as to increase yield and stabilise operation.

Figure 15 illustrates a drive circuit for a data line of an active matrix assembly according to the present invention. A plurality of shift register cells 186 are provided, each shift register cell comprising a bootstrap capacitor 188, transistors 189, 191 and a reset transistor 190 for selecting a shift register. A start pulse SP (Figure 16) is applied *via* an input gate 187 to an initial shift register cell. Outputs S_1 to S_m from the shift register cells were applied to sampling and holding transistors H_1 to H_m. In synchronism with a scanning signal, video input V, S (a video signal or data writing signal) is caused to be sampled and held in each of parasitic capacitors CG_1 to CD_m on the data line. Since the drive circuit for the data line performs all operations in one scanning line, it operates at a high speed with substantially no concern over leakage current. However, care should be taken to maintain high-speed operation and minimise power consumption which tends to be increased due to high-speed operation.

The shift register cells have a level of "1" only at one out of *m* bits, and hence power consumption is small unless it is clocked. The sampling and holding transistors H_1 to H_m are required to effect high-speed switching. Such a requirement can be met as their gates are supplied with inputs which have an amplitude about twice that of the clock signal due to bootstrap operation as shown in Figure 16.

Figure 17 is a circuit diagram of a complete active matrix assembly according to the present invention comprising data shift registers 198, 199, dummy cells 194, 195 for producing return signals at final stages, and sampling and holding transistors H_1 to H_m, the arrangement being symmetrical with respect to a horizontal centre line. Gate shift registers 192, 193 and dummy cells 196, 197 are located symmetrically with respect to a vertical centre line. The peripheral circuit may not be symmetrical and only one half may be provided. As illustrated, however, a plurality of rows, that is, two rows, of shift registers are provided for the sake of yield. Four or eight rows of shift registers may well serve the purpose.

With the active matrix assembly shown in Figure 17 being composed of transistors that are constructed of thin films of silicon in the manner discussed above, the following advantages result. Since, on the data line side, the clock frequency is high (several MHz) power consumption is greater due to parasitic capacitance on the clock line than due to the shift registers. More specifically, with transistors constructed by the bulk silicon process, capacitance on the clock line and capacitance at the junction with the substrate would amount to 100 PF or more, resulting in a reduction in speed of clock pulses and power consumption of 10 mA or more. However, the substrate used in the present invention has a parasitic capacitance of only several PF, and greatly reduces down power consumption and increases operational speed. Transistors constructed by bulk silicon process have a increased threshold voltage due to a back gate effect if the potential at the source of the transistor 182 of Figure 13 is increased. As a result, it is necessary to raise the voltage at the gate T_1 of the transistor 182 in order to obtain a required signal voltage, with the result that either the level of the clock signal has to be increased or the bootstrap capacitor 185 has to occupy a considerably larger area. With transistors constructed of thin films of silicon, however, the transistor substrate floats without giving rise to a back gate effect and hence the clock amplitude may be reduced with resulting lower power consumption, and the bootstrap capacitor may be small requiring a reduced area therefor. The bootstrap capacitors in the drive circuit are formed basically of isolation films between the

gates and channels of the transistors, a feature which is different from the capacitors 3. The bootstrap capacitor should have an inter-electrode capacitance variable by the voltage at the gate or upper electrode. To that end, the lower electrode of the capacitor is made of a thin film of silicon which is doped lightly or is not doped at all.

Simultaneous formation of the active matrix assemblies and the drive circuits with the thin film of silicon on the insulating substrate allows easy connecting wiring and renders the entire assembly less costly. Since the drive circuits comprise non-inverting ratioless shift registers as shown in Figures 13 and 15, with parasitic capacitance being reduced to a large extent, a reduction in the overall power consumption, an increased yield, and a reduced cost are obtainable.

Where the transparent substrate is under the control of a transparent liquid crystal drive, FE-type liquid crystal segments can be used which provide a maximum degree of contrast, so that the display has an increased degree of brightness and improved quality. Where the substrate is made of glass or a similar material, the display device or panel can be assembled with ease, yield of assembly is increased and is simplified compared to active matrix assemblies constructed using conventional bulk silicon processes. With the peripheral drive circuits on the same substrate as the active matrix assembly, a great reduction in power consumption results.

Claims

1. An active matrix assembly including a thin layer of silicon which defines a channel region.

2. An assembly as claimed in claim 1 including a first thin layer of silicon, a first insulating layer on said first layer of silicon, and a second thin layer of silicon.

3. An assembly as claimed in claim 1 or 2 in which said first and second layers of silicon constitute a channel region and a gate, respectively, of a transistor.

4. An assembly as claimed in claim 1 or 2 in which said first and second layers of silicon constitute a gate and a channel region, respectively, of a transistor.

5. An assembly as claimed in claim 3 or 4 in which said first insulating layer constitutes a dielectric of a capacitor, and said first and second layers of silicon constitute electrodes of the capacitor.

6. An assembly as claimed in claim 3 including a second insulating layer on said second layer of silicon and wiring material on said second insulating layer, said second insulating layer constituting a dielectric of a capacitor, said second layer of silicon and said wiring material constituting electrodes of the capacitor.

7. An assembly as claimed in any of claims 2 to 5 in whichsaid assembly is formed by a low temperature process at a temperature of 600°C or less, said first insulating layer comprising an oxide film formed by an O_2 plasma technique.

8. An assembly as claimed in claim 6 in which said assembly is formed by a low temperature process at a temperature of 600°C or less, said first and/or second insulating layer comprising an oxide film formed by an O_2 plasma technique.

9. An assembly as claimed in any preceding claim in which said layer of silicon which defines the channel region is locally annealed by a laser beam or electron beam.

10. An assembly as claimed in any preceding claim in which said layer of silicon which defines the channel region is formed by a reduced pressure chemical vapour deposition technique at a temperature of 600°C or less.

11. An assembly as claimed in any preceding claim in which said layer of silicon which defines the channel region has a thickness of 3,700 Å or less.

12. An assembly as claimed in any preceding claim including a transparent substrate and a transparent liquid crystal driving electrode on said transparent substrate.

13. An assembly as claimed in claim 12 including wiring material for a data line, said transparent liquid crystal driving electrode being made of a material which is the same as said wiring material.

14. An assembly as claimed in claim 12 in which said transparent liquid crystal driving electrode is made of a Si_nO_2 film, a metal film having a thickness of 500 Å or less, or a thin film of silicon.

15. An assembly as claimed in any of claims 1 to 5 in which said assembly is formed by a high temperature process at a temperature of 600°C or higher, said first insulating layer comprising a thin thermal oxide film of silicon.

16. An assembly as claimed in claim 6 in which said assembly is formed by a high temperature process at a temperature of 600°C or higher, said first and/or second insulating layer comprising said first and/or second layer of silicon respectively which has been thermally oxidised.

17. An assembly as claimed in claim 12 including a liquid crystal segment drivable in a twisted nematic mode.

18. An assembly as claimed in any preceding claim including a substrate on which the active matrix assembly is formed together with at least one peripheral drive circuit, said at least one peripheral drive circuit including non-inverting ratioless shift registers.

19. An active matrix assembly substantially as herein described with reference to and as shown in Figures 3 to 17 in the accompanying drawings.

20. An active matrix assembly comprising a thin film of silicon which defined a channel.

21. An active matrix assembly comprising a first thin film of silicon, a first insulation film on said first thin film of silicon, and a second thin film of silicon.

22. An active matrix assembly comprising a first thin film of silicon, a first insulation film on said first thin film of silicon, and a second thin film of silicon on said first insulation film, said first and

second thin films of silicon constituting a channel and a gate, respectively, of a transistor.

23. An active matrix assembly comprising a first thin film of silicon, a first insulation film on said first thin film of silicon, and a second thin film of silicon on said first insulation film, said first and second thin films of silicon constituting a gate and a channel, respectively, of a transistor.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1982. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.